CLAIMS

What is claimed is:

1. An execution unit in a microprocessor, the execution unit comprising:
look-up memory; and
a first circuit coupled to the look-up memory,
the first circuit, in response to the microprocessor receiving a first instruction, partitioning the look-up memory into a first plurality of look-up tables,
the first circuit, in response to the microprocessor receiving a second instruction, partitioning the look-up memory into a second plurality of look-up tables which are different from the first plurality of look-up tables.

2. An execution unit as in claim 1 wherein a total number of bits used by each entry in the first plurality of look-up tables is different from a total number of bits used by each entry in the second plurality of look-up tables; and wherein the microprocessor is a media processor formed in a monolithic semiconductor substrate, which comprises a memory controller for controlling DRAM memory, said media processor being coupled to said memory controller.

3. An execution unit as in claim 1 wherein a total number of entries in each of the first plurality of look-up tables is different from a total number of entries in each of the second plurality of look-up tables.

4. An execution unit as in claim 1 wherein the look-up memory comprises a plurality of look-up units, and wherein the first circuit configuring the plurality of look-up units into a third plurality of look-up tables in response to the microprocessor receiving a third instruction.

5. An execution unit as in claim 4 wherein each of the third plurality of look-up units contains 256 8-bit entries.

6. An execution unit as in claim 4 wherein a total number of entries in each of the third plurality of look-up tables is one of:

a) 256;

b) 512; and

c) 1024.

7. An execution unit as in claim 4 wherein a total number of bits used by each entry in the third plurality of look-up tables is one of:

a) 8;

b) 16; and

c) 24.

8. An execution unit as in claim 1 further comprising:
a second circuit coupled to the look-up memory, the second circuit configured to receive a plurality of numbers, in response to the microprocessor receiving the first instruction, the first plurality of look-up tables looking up simultaneously a plurality of entries, each of the plurality of entries being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers.

9. An execution unit as in claim 1 further comprising:
a second circuit coupled to the look-up memory, the second circuit configured to receive a string of bits, in response to the microprocessor receiving the first instruction,
the second circuit generating a plurality of indices using a plurality of segments of bits in the string of bits,
the first plurality of look-up tables looking up simultaneously a plurality of entries, each of the plurality of entries being in one of the plurality of look-up tables and being pointed to by one of the plurality of indices.

10. An execution unit as in claim 9 further comprising:
a third circuit coupled to the look-up memory, the third circuit combining the plurality of entries into a first result.

11. An execution unit as in claim 10 further comprising:

a forth circuit coupled to the second circuit, the forth circuit configured to receive a plurality of data elements specifying the plurality of segments in the string of bits.

12. An execution unit as in claim 10 further comprising:

a fifth circuit coupled to the second circuit, the fifth circuit configured to receive at least one format; and

a sixth circuit coupled to the fifth circuit and the third circuit, in response to the microprocessor receiving the first instruction,

the fifth circuit formatting the string of bits into at least one escape data using the at least one format, and

the sixth circuit combining the at least one escape data with the first result into a second result.

13. A processing system comprising an execution unit as in claim 1.

14. A microprocessor execution unit comprising:

a plurality of look-up tables;

a first circuit configured to accept a first plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each

of the plurality of entries being in one of the plurality of look-up tables

a second circuit configured to accept a second plurality of numbers; and

a third circuit coupled to the first circuit, the second circuit, and the plurality of look-up tables, the third circuit, in response to the microprocessor receiving a single instruction, replacing simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers.

15. A processing system comprising an execution unit as in claim 14.

16. An execution unit in a microprocessor, the execution unit comprising:

a plurality of look-up tables;

a first circuit coupled to the plurality of look-up tables and a Direct Memory Access (DMA) controller, the first circuit, in response to the microprocessor receiving a single instruction, replacing at least one entry in at least one of the plurality of look-up tables with at least one data element using the DMA controller.

17. A processing system comprising an execution unit as in claim 16.

18. An execution unit in a microprocessor, the execution unit comprising:

a plurality of look-up tables;

a first circuit coupled to the plurality of look-up tables and a Direct Memory Access (DMA) controller, the first circuit, in response to the microprocessor receiving a single instruction, replacing at least one entry for each of the plurality of look-up tables with a plurality of data elements using the DMA controller.

19. A processing system comprising an execution unit as in claim 18.

20. An execution unit in a microprocessor comprising:
a plurality of look-up tables;
a first circuit coupled to the plurality of look-up tables, the first circuit configured to receive a string of bits;
a second circuit coupled to the plurality of look-up tables and the first circuit, the second circuit configured to receive a plurality of data elements, in response to the microprocessor receiving a single instruction, the second circuit generating a plurality of indices using the plurality of data elements and the string of bits, the plurality of look-up tables looking up simultaneously a plurality of entries using the plurality of indices; and
a third circuit coupled to the plurality of look-up tables, the third circuit combining the plurality of values into a first result.

21. An execution unit as in claim 20 further comprising:

a fifth circuit coupled to the second circuit, the fifth circuit configured to receive at least one format; and

a sixth circuit coupled to the fifth circuit and the third circuit, in response to the microprocessor receiving the single instruction,

the fifth circuit formatting the string of bits into at least one escape data using the at least one format, and

the sixth circuit combining the at least one escape data with the first result into a second result.

22. A processing system comprising an execution unit as in claim 21.

23. An execution unit in a microprocessor, the execution unit comprising:

means for receiving a first plurality of numbers and a second plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables; and

means for replacing simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers;

wherein the above means operate in response to the microprocessor receiving a single instruction.

24. An execution unit as in claim 23 wherein the first plurality of numbers are received from a first entry in a register file; and the second plurality of numbers are received from a second entry in the register file.

25. An execution unit as in claim 24 wherein the single instruction specifies indices of the first and second entries in the register file.

26. An execution unit in a microprocessor, the execution unit comprising:
means for replacing at least one entry in at least one of a plurality of look-up units in a microprocessor unit with at least one number using a Direct Memory Access (DMA) controller;
wherein the above means operate in response to the microprocessor receiving a single instruction.

27. An execution unit in a microprocessor, the execution unit comprising:
means for replacing at least one entry for each of a plurality of look-up units in a microprocessor with a plurality of numbers using a Direct Memory Access (DMA) controller;
wherein the above means operate in response to the microprocessor receiving a single instruction.

28. An execution unit as in claim 27 wherein a single index encoded in the instruction specifies a location of the at least one entry in the plurality of look-up units.

29. An execution unit as in claim 27 wherein a single index encoded in the instruction specifies a total number of the at least one entry for each of a plurality of look-up units.

30. An execution unit as in claim 27 wherein a source address of the plurality of numbers is specified in an entry of a register file.

31. An execution unit as in claim 30 wherein the single instruction specifies an index of the entry in the register file.

32. An execution unit as in claim 27 wherein an identity number encoded in the single instruction specifies the DMA controller.

33. An execution unit in a microprocessor, the execution unit comprising:
means for receiving a plurality of numbers;
means for partitioning look-up memory into a plurality of look-up tables;
means for looking up simultaneously a plurality of elements from the plurality of look-up tables, each of the plurality of elements being in

one of the plurality of look-up tables and being pointed to by one of the plurality of numbers;

wherein the above means operate in response to the microprocessor receiving a single instruction.

34. An execution unit as in claim 33 wherein the means for receiving a plurality of numbers comprises:

means for partitioning a string of bits into a plurality of segments to generate the plurality of numbers.

35. An execution unit as in claim 34 wherein the single instruction specifies format information in which the plurality of numbers are stored in the string of bits.

36. An execution unit as in claim 33 wherein the look-up memory comprises a plurality of look-up units, and wherein the means for partitioning look-up memory comprises:

means for configuring the plurality of look-up units into the plurality of look-up tables.

37. An execution unit as in claim 33 wherein the string of bits is received from an entry of a register file.

38. An execution unit as in claim 37 wherein the single instruction specifies an index of the entry.

39. An execution unit as in claim 33 further comprising:
means for storing the plurality of elements in an entry of a register file.

40. An execution unit as in claim 39 wherein the single instruction specifies an index of the entry.

41. An execution unit as in claim 39 wherein the single instruction specifies format information in which the plurality of elements are stored in the entry.

42. An execution unit as in claim 36 wherein each of the plurality of look-up units comprises 256 8-bit entries.

43. An execution unit as in claim 33 wherein the single instruction specifies a total number of entries contained in each of the plurality of look-up tables.

44. An execution unit as in claim 43 wherein the total number of entries is one of:
a) 256;
b) 512; and

c) 1024.

45. An execution unit as in claim 33 wherein the single instruction specifies a total number of bits used by each entry contained in the plurality of look-up tables.

46. An execution unit as in claim 45 wherein the total number of bits is one of:
a) 8;
b) 16; and
c) 24.

47. An execution unit in a microprocessor, the execution unit comprising:
means for receiving a string of bits;
means for generating a plurality of indices using a plurality of segments of bits in the string of bits;
means for looking up simultaneously a plurality of entries from a plurality of look-up tables using the plurality of indices; and
means for combining the plurality of entries into a first result;
wherein the above means operate in response to the microprocessor receiving a single instruction.

48. An execution unit as in claim 47 wherein further comprising:

means for receiving a plurality of data elements specifying the plurality of segments in the string of bits.

49. An execution unit as in claim 48 wherein the plurality of data elements are received from an entry in a register file.

50. An execution unit as in claim 49 wherein the single instruction specifies an index of the entry in the register file.

51. An execution unit as in claim 48 further comprising:
means for receiving a bit pointer, wherein the plurality of segments in the string of bits are determined using the bit pointer and the plurality of data elements.

52. An execution unit as in claim 51 further comprising:
means for generating a new bit pointer using the first result.

53. An execution unit as in claim 47 further comprising:
means for receiving an offset, wherein the plurality of indices are determined using the offset and the plurality of segments of bits.

54. An execution unit as in claim 47 further comprising:

means for partitioning look-up memory into the plurality of look-up tables before said looking-up.

55. An execution unit as in claim 54 wherein the look-up memory comprises a plurality of look-up units, and wherein the means for partitioning look-up memory comprises:
means for configuring the plurality of look-up units into the plurality of look-up tables.

56. An execution unit as in claim 69 wherein each of the plurality of look-up units comprises 256 8-bit entries.

57. An execution unit as in claim 47 wherein the single instruction specifies a total number of entries contained in each of the plurality of look-up tables.

58. An execution unit as in claim 57 wherein the total number of entries is one of:
a) 256;
b) 512; and
c) 1024.

59. An execution unit as in claim 47 wherein the single instruction specifies a total number of bits used by each entry contained in the plurality of look-up tables.

60. An execution unit as in claim 59 wherein the total number of bits is one of:
a) 8;
b) 16; and
c) 24.

61. An execution unit as in claim 54 wherein the plurality of look-up tables are configure according to an indicator in an entry in a register file.

62. An execution unit as in claim 61 wherein the single instruction specifies an index of the entry in the register file.

63. An execution unit as in claim 47 wherein the means for combining the plurality of entries comprises:
means for selecting a valid data from the plurality of entries.

64. An execution unit as in claim 63 further comprising:
means for generating an indicator indicating whether none of the plurality of entries is valid.

65. An execution unit as in claim 63 wherein the valid data is selected according to priorities of the look-up tables from which the plurality of entries are looked up.

66. An execution unit as in claim 63 wherein the means for combining the plurality of entries further comprises:
means for formatting the valid data according to a type of the valid data.

67. An execution unit as in claim 66 wherein the type of the valid data is one of:
a) zero fill;
b) sign magnitude; and
c) two complement.

68. An execution unit as in claim 67 further comprising:
means for retrieving a sign bit from the string of bits for the valid data,
wherein the first result is obtained by formatting the valid data using the sign bit when the type of the valid data is sign magnitude.

69. An execution unit as in claim 47 wherein an entry in the plurality of entries contains:
a) information indicating whether the entry is valid;
b) information indicating a type of the entry; and

c) information indicating a number of bits of a code word to be decoded.

70. An execution unit as in claim 47 wherein the string is received from an entry in a register file.

71. An execution unit as in claim 70 wherein the single instruction specifies an index of the entry in the register file.

72. An execution unit as in claim 47 further comprising:
means for receiving a first number indicating a position of a last bit of input in the string of bit.

73. An execution unit as in claim 72 further comprising:
means for generating an indicator indicating whether any bit after the last bit of input is used in obtaining the first result.

74. An execution unit as in claim 58 further comprising:
means for generating an indicator indicating whether one of the plurality of segments of bits contains a predetermined code.

75. An execution unit as in claim 74 wherein the predetermined code represents an end of block condition.

1 76. An execution unit as in claim 47 further comprising:
2 means for receiving at least one format;
3 means for formatting the string of bits into at least one escape data according
4 to the at least one format; and
5 means for combining the at least one data and the first result into a second
6 result.

1 77. An execution unit as in claim 76 wherein one of the at least one format is for
2 data of a type which is one of:
3 a) zero fill;
4 b) sign magnitude; and
5 c) two complement.

1 78. An execution unit as in claim 76 wherein the at least one format is received
2 from an entry of a register file.

1 79. An execution unit as in claim 78 wherein the single instruction specifies an
2 index of the entry in the register file.